ABSTRACT OF THE DISCLOSURE

An interconnect structure for microelectronic devices includes a plurality of patterned, spaced apart, substantially co-planar, conductive lines, a first portion of the plurality of conductive lines having a first intralayer dielectric of a first dielectric constant therebetween, and a second portion of the plurality of conductive lines having a second intralayer dielectric of a second dielectric constant therebetween. By providing in-plane selectability of dielectric constant, in-plane decoupling capacitance, as between power supply nodes, can be increased, while in-plane parasitic capacitance between signal lines can be reduced.